

ABSTRACT

In the present invention a method is shown that uses three concurrent word line voltages in memory cell operations of an a NOR type EEPROM flash memory array. A first concurrent word line voltage controls the operation on a selected word line within a selected memory block. The second concurrent word line voltage inhibits cells on non selected word lines in the selected memory block, and the third concurrent word line voltage inhibits non-selected cells in non-selected blocks from disturb conditions. In addition the three consecutive word line voltages allow a block to be erased, pages within the block to be verified as erased, and pages within the block to be inhibited from further erasure. The three consecutive voltages also allow for the detection of over erasure of cells, correction on a page basis, and verification that the threshold voltage of the corrected cells are above an over erase value but below an erased value. The methods described herein produce a cell threshold voltage that has a narrow voltage distribution.